Remarks

Thorough examination by the Examiner is noted and appreciated.

Examiner has previously indicated allowance of claims 11-20, and now has rejected claims 11-18 and 20, indicating claim 19 is allowable, and citing new art not previously or record, and without comment, except that the previous rejection has been withdrawn. See e.g., MPEP 706.04

> A claim noted as allowable shall thereafter be rejected only after the proposed rejection has been submitted to the primary examiner for consideration of all the facts and approval of the proposed action. Great care should be exercised in authorizing such a rejection. See *Ex parte Grier*, 1923 C.D. 27, 309 O.G. 223 (Comm'r Pat. 1923); *Ex parte Hay*, 1909 C.D. 18, 139 O.G. 197 (Comm'r Pat. 1909).
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> Because it is unusual to reject a previously allowed claim, the examiner should point out in his or her office action that the claim now being rejected was previously allowed by using Form Paragraph 7.50.

Applicants acknowledge Examiners indication of allowable subject matter in claim 19. The claims have been amended to

achieve allowable subject matter and to further clarify Applicants invention as well as include aspects of limitations included in claim 19 in a good faith attempt to achieve allowable subject matter in all the claims.

Support for the amended and newly added claims are found in the original claims and/or the Specification. No new matter has been added.

For example see paragraph 0025:

Referring to FIG. 2F, in another aspect of the invention, **following the reverse tone patterning process** including development of the resist, **a dummy pattern is added to unpatterned resist portion** e.g., 32C **between the active area including STI trench 31B and the inactive area trench 31C overlying the laser mark area 28**. For example, following the reverse tone patterning process, an additional dummy pattern mask, according to preferred embodiments, is interposed between the reverse tone pattern mask and the process wafer surface to allow proper re-alignment of the reticle (mask) over the desired wafer exposure area, e.g., a one shot exposure of resist portion 32C, while avoiding shadowing (shielding) effects from the reverse tone pattern mask during exposure. Following exposure and development of the resist layer portion 32C, dummy pattern resist portions e.g., 32D and 32E are formed in the resist layer as shown in an exemplary embodiment, while leaving a portion of resist layer portion e.g., 32C overlying the trench 31C, which at least partially, preferably substantially completely, overlies the laser mark area 28.

Claim Rejections under 35 USC 103

Claims 1-18, 20 and 33-40 stand rejected under 35 USC 103(a) as being unpatentable over Uchiyama (US 6,603,162) in view Yu (US 5,911,110) and of Applicants alleged admitted prior art.

Uchiyama discloses a method for **overcoming the problem of dishing in an optical pattern recognition area** formed in a scribe region (see Abstract; col 2, lines 24-51). In the method of Uchiyama a dummy pattern is formed in scribe region (see Figure 3) where the **dummy pattern is etched into the substrate at the same time isolation features** (shallow trench) are formed in the active region (see item 5, Figures 8A, 8B; col 9, lines 49-col 10, line 24). Uchiyama discloses that the photoresist may be left in place or may be removed as shown in the figures, and the silicon nitride layer (3) used as a hard mask **during etching of the trenches**. The trenches are then backfilled with oxide (6, Figure 9) which is then planarized by CMP (Figure 10) **without any intervening etching (removal) of the oxide**. Uchiyama teaches that dishing is improved with respect to the product region (PR)

and the target region (where optical recognition pattern will later be formed) (col 10, lines 9-24).

On the other hand, Yu discloses a method for improving an shallow trench isolation (STI) formation process where dry etching following formation of a **reverse tone etching mask with a dummy pattern** on the STI oxide is performed prior to CMP to remove portions of the STI oxide to form STI oxide reverse tone pattern and dummy structures (**over large featureless area**) to avoid a micro-loading effect during etching (see col 3, lines 16-24). The method of Yu **overcomes the problem of leaving residual oxide on large oxide areas due to a slower etching rate** (micro-loading effect) where the residual oxide is not removed (planarized) by a subsequent CMP process (see col 2, lines 1-8).

Yu overcomes the micro-loading effect during the etching process by using a **reverse tone mask pattern with a dummy mask pattern** (col 4, lines 15-17; col 4, lines 55-65) on the STI oxide including over large oxide areas **or using a replacement mask pattern** (to replace reverse tone mask with dummy pattern) to form patterned structures over the entire process wafer surface (see item 34, Figure 6; col 4, lines 15-38) (**i.e., a one mask/patterning process**), followed by etching the STI oxide

(trench filling layer), **then followed by stripping the reverse tone pattern and the dummy pattern formed during the etching process** (Figure 7, col 4, lines 64-col 5, line 17; col 5, lines 9-12) and **then performing a CMP process (following stripping of the dummy structures)**.

There is no apparent motivation to combine the disparate teachings of Yu, who teaches etching away a portion of an STI oxide layer by dry etching according to a reverse tone mask with a dummy pattern over small and large oxide areas **to solve the problem of different dry etching rates (micro-loading) during the etching process**, then **removing the resulting STI oxide dummy patterns prior to performing (CMP)** with Uchiyama, who teaches etching dummy trench (STI) structures (into the substrate) including forming dummy trenches **in a scribe area** of the wafer followed by backfilling with STI oxide, then followed by CMP **(no intervening etching step) to overcome the problem of CMP dishing in a scribe area (optical target area)** of a process wafer.

The fact that Applicants disclose that it is conventional to form a laser marked identification area **at the periphery of a wafer** and further disclose that a **problem presented thereby is a step height** that is created in prior art processes between the

laser marked identification area and adjacent active areas cannot further help Examiner in producing Applicants disclosed and claimed invention or make out a *prima facie* case of obviousness.

The only motivation for combining the disparate teachings of Yu and Uchiyama, who discuss different processes and different dummy structures to overcome different problems can only be impermissibly found in Applicants disclosure.

Neither Uchiyama nor Yu recognize or provide a solution to the problem that Applicants have recognized and solved by their disclosed and claimed invention:

"A method for avoiding a step height over a readable laser marked portion of a process wafer"

Even assuming *arguendo* a proper motivation for combining teachings of Uchiyama and Yu with the teaching by Applicants that laser marks are commonly put at the periphery of a wafer, such combination does not produce Applicants disclosed and claimed invention including those item in **bold type**:

" **A method for avoiding a step height over a readable laser marked portion of a process wafer** comprising the steps of:

providing a process wafer comprising active area trenches and **at least one inactive area trench formed overlying at least a portion of a laser marked portion at the process wafer periphery;**

forming a filling layer over the active area trenches and the at least one inactive area trench to substantially fill the respective trenches;

forming a resist layer comprising **first patterned portions and second patterned portions**, said first patterned portions overlying the active area and second patterned portions disposed between the active area and the inactive area, **said first and second patterned portions formed separately from one another;**

removing the filling layer portions not covered by the resist layer;

removing the resist layer to expose remaining filling layer portions; and,

planarizing the wafer process surface **including removing said remaining filling layer portions** according to chemical

mechanical polish (CMP) process wherein the active area trenches and the at least one inactive area trench **including said laser marked portion** are substantially co-planar."

For example, as pointed out above, **Yu discloses stripping the dummy structures after etching and prior to performing a CMP** process, while Uchiyama **does not teach an etching process (removal of filling layer) to form dummy structures** in the filling layer prior to a CMP process.

The cited references further fail to show additional limitations in independent claims 11, 33, and 37, and therefore in dependent claims.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

Applicants acknowledge Examiners indication of allowable subject matter in claim 19. The claims have been amended to achieve allowable subject matter and to further clarify Applicants invention as well as include aspects of limitations included in claim 19 in a good faith attempt to achieve allowable subject matter in all the claims.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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